In The Claims

Applicant submits below a complete listing of the current claims, with insertions, if any, indicated by underlining and deletions, if any, indicated by strikeouts and/or double bracketing.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

Please cancel claims 1.-3.

4. (Currently amended) A circuit for regenerating a clock signal based on two complementary signals by means of a D flip-flop, a clock input of which receives the result of a logic combination of two shaping signals resulting from a filtering of the respective rising edges of the complementary signals, wherein a reset input of the flip-flop receives one of said shaping signals,

wherein the logic combination is of NAND type, the shaping signals being provided by inverters, and

wherein the reset input of the flip-flop is connected at the output of one of the inverters for shaping the complementary signal, of which an output of the flip-flop provides an inverted image.

Please cancel claims 5 - 6.

7. (Previously Presented) An interface system between a modem and a transmission line, of the type using a capacitive isolation barrier to transmit a clock for modulating the signals to be transmitted from the modem to a processing circuit on the transmission line side of the interface system, including the clock regeneration circuit of claim 4.

8. (Previously Presented) A clock signal regeneration circuit, comprising:

a first input for a clock signal and a second input for an inverted clock signal;

logic to shape the clock signal into a first signal and the inverted clock signal into a second signal;

a flip-flop; [and]

means for setting an initial state of the flip-flop after each alternate edge of the second signal,

further comprising a NAND gate, wherein the first signal and the second signal are input to the NAND gate

wherein the flip-flop is a D-type flip-flop, and

wherein an output of the NAND gate is input to a clock input of the flip-flop.

9. (Previously Presented) The clock signal regeneration circuit of claim 8, wherein the clock signal regeneration circuit is located on a line side of a capacitive isolation barrier.

10. (Previously Presented) The clock signal regeneration circuit of claim 8, wherein the means for setting an initial state of the flip-flop comprises means for setting the initial state of the flip-flop after each rising edge of the second signal.

11. (Previously Presented) The clock signal regeneration circuit of claim 8, wherein the flip-flop comprises a reset input, and wherein one of the first signal and the second signal is coupled to the reset input.

12. (Previously Presented) The clock signal regeneration circuit of claim 8, wherein the logic comprises means for detecting each alternate edge of the clock signal and shaping the clock signal into a first signal having a single voltage pulse between each alternate edge of the clock signal, and means for detecting each alternate edge of the inverted clock signal and shaping the inverted clock signal into a second signal having a single voltage pulse between each alternate edge of the inverted clock signal.

13. (Previously Presented) The clock signal regeneration circuit of claim 12, wherein the logic comprises means for detecting each rising edge of the clock signal and shaping the clock signal into a first signal having a single voltage pulse between each rising edge of the clock signal, and means for detecting each rising edge of the inverted clock signal and shaping the inverted clock signal into a second signal having a single voltage pulse between each rising edge of the inverted clock signal.

14. (Previously Presented) The clock signal regeneration circuit of claim 8, wherein the logic comprises:

first and second resistors connected between the clock signal and the inverted clock signal;

a first capacitor coupled to the first clock signal and the first resistor; and

a second capacitor coupled to the inverted clock signal and the second resistor.

15. (Previously Presented) The clock signal regeneration circuit of claim 14, wherein a reference voltage is coupled between the first and second resistors.

16. (Previously Presented) The clock signal regeneration circuit of claim 14, further comprising a first inverter coupled to the first capacitor and a second inverter coupled to the second capacitor.

17. (Previously Presented) The clock signal regeneration circuit of claim 16, wherein the output of the first inverter is the first signal and the output of the second inverter is the second signal.

18 – 19 Cancelled.

20. (Currently amended) The clock signal regeneration circuit of claim ~~19~~ 8, wherein the flip-flop comprises a reset input, and wherein the second signal is coupled to the reset input.

21. (Currently amended) A method of regenerating a clock signal, comprising acts of:

shaping a clock signal into a first signal and an inverted clock signal into a second signal; and

setting an initial state of a flip-flop after each alternate edge of the second signal, wherein the flip-flop is coupled to the first and second signals,

further comprising an act of inputting the first and second signals to a NAND gate, wherein the flip-flop is a D-type flip-flop, and

wherein the method further comprises an act of inputting an output of the NAND gate to a clock input of the flip-flop..

22. (Previously Presented) The method of claim 21, wherein the acts of regenerating the clock signal are performed on a line side of a capacitive isolation barrier.

23. (Previously Presented) The method of claim 21, wherein the act of setting the initial state of the flip-flop comprises setting the initial state of the flip-flop after each rising edge of the second signal.

24. (Previously Presented) The method of claim 21, wherein the act of setting the initial state of the flip-flop comprises coupling one of the first signal and the second signal to a reset input of the flip-flop.

25. (Previously Presented) The method of claim 21, wherein the act of shaping comprises:

detecting each alternate edge of the clock signal and shaping the clock signal into a first signal having a single voltage pulse between each alternate edge of the clock signal; and

detecting each alternate edge of the inverted clock signal and shaping the inverted clock signal into a second signal having a single voltage pulse between each alternate edge of the inverted clock signal.

26. (Previously Presented) The method of claim 21, wherein the act of shaping comprises:

detecting each alternate edge of the clock signal and shaping the clock signal into a first signal having a single voltage pulse between each rising edge of the clock signal; and

detecting each alternate edge of the inverted clock signal and shaping the inverted clock signal into a second signal having a single voltage pulse between each rising edge of the inverted clock signal.

27. (Previously Presented) The method of claim 21, wherein the act of shaping includes shaping the first and second signals between ground and a reference potential.

28 – 29 Cancelled

30. (Currently amended) The method of claim ~~29~~ 21, wherein the flip-flop comprises a reset input, and wherein the method further comprises an act of inputting the second signal to the reset input.